MEGAWATT HIGH SPEED SOLID STATE CIRCUIT BREAKER FOR PULSE POWER APPLICATIONS

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ABSTRACT

Two 3.3 Megawatt 3 phase 4160 V solid state circuit breakers, which can interrupt full current within 300 microseconds, have been installed on the 6.6 Megawatt power supply at the Army Pulse Power Center at Fort Monmouth. These devices, utilizing Gate Turnoff Thyristors (GTOs), can interrupt two orders of magnitude faster than standard mechanical contact type circuit breakers. The system also includes a personal computer based power supply control and data acquisition system, with over seventy data channels and the capability to operate unattended. This system will make possible pivotal evaluation of megawatt class pulse power components under the most severe conditions, since it will be possible to run said experimental components at their limits and still protect them from fault damage and destruction, while measuring operating parameters even at the point of the fault.

Introduction

In the evaluation of pulse power components and networks, under fault conditions, the tens of milliseconds required by a mechanical circuit breaker to clear is an eternity. It was thus planned that a new type of circuit breaker, utilizing solid state technology, be installed on one of the multimegawatt power supplies at the U.S. Army Pulse Power Center at Fort Monmouth, NJ. The requirements of such circuit breakers are listed in Table 1. Note that an opening time of less than 300 microseconds is specified. This is two orders of magnitude less than a comparable mechanical circuit breaker.

TABLE 1

SOLID STATE CIRCUIT BREAKER TECHNICAL REQUIREMENTS

Withstand Voltage-Terminals	15 kV
Withstand Voltage to Ground	15 kV
BIL (Basic Impulse Level)	30 kV
Maximum Interrupt Current	2 kA
Surge Current (10 ms-1 cycle)	10 kA
Steady State Switch Impedance	50 mOhms
Closing Time	50 μs
Opening Time	300 μs
Operating Temperature	0-40 °C

The project was begun in 1989. By the beginning of 1993, two solid state circuit breakers were installed on the dual 3.3 Megawatt (6.6 Megawatt combined) power supply at Fort Monmouth. They are now functional.

Solid State Circuit Breaker

The solid state circuit breakers were designed and built by the Westinghouse Science and Technology Center, Pittsburgh, PA. They utilize Gate Turnoff Thyristors (GTOs) as power control elements. The circuit breakers are designed for three phase, 4160 V operation and are installed in the power mains of the above mentioned 6.6 Megawatt power supply. The installed circuit breakers are shown in Figure 1. The units are in a climatically controlled enclosure and are air cooled. The pulse current rating for each circuit breaker is 500 Arms for 100 seconds duration, with five minutes between successive operations. Continuous current rating is 93 Arms, which is consistent with the operational parameters of the 6.6 Megawatt power supply.

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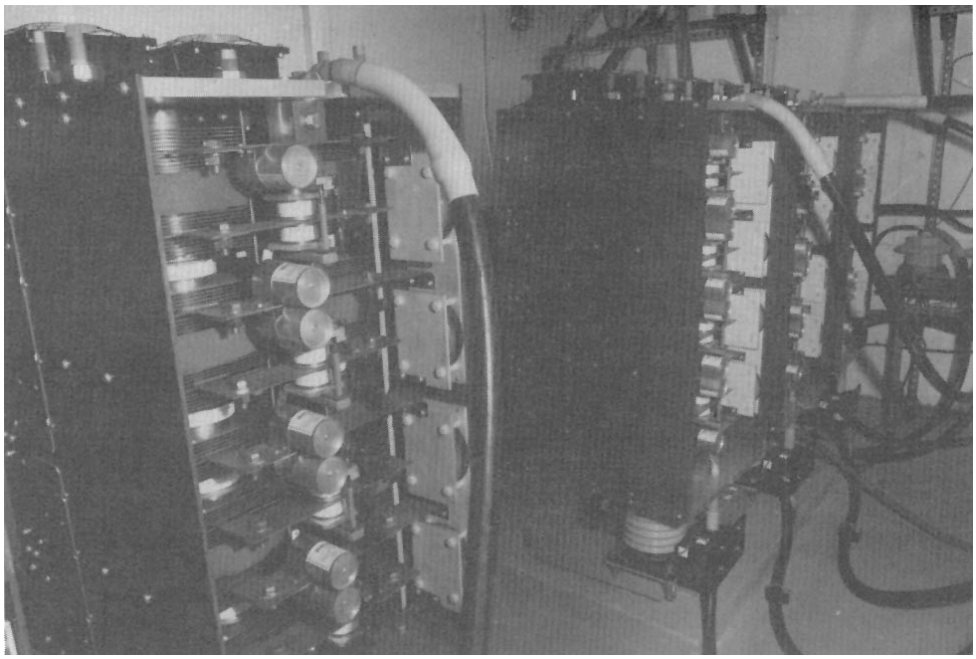

Figure 1. Two 3.3 megawatt solid state circuit breakers installed at the U.S. Army Pulse Power Center, Fort Monmouth, NJ. A single phase of one circuit breaker (at left) shows GTO snubber capacitors (cylinders), snubber diodes (small white presspacks) at center and GTOs (large white presspacks) to the left of the snubber networks. Note cooling fans at the tops of the units.

The solid state circuit breaker will limit and interrupt the instantaneous load current to less than 2 kA for all fault conditions, including a short circuit fault on the output bus of the solid state circuit breaker. The current trip level is adjustable up to 1.5 kA. The solid state circuit breaker provides soft start voltage control of the output voltage to the load during the initial closing of the power mains, in order to limit the in-rush current to the load. The current limit level during this soft start mode is adjustable up to 500 A.

Each phase of the three-phase solid state circuit breaker consists of four sets of antiparallel GTOs connected in series, as shown in Figure 2. This antiparallel configuration is necessary, since GTOs are unidirectional devices and one device is necessary for each half cycle. One GTO in each of the four sets conducts current in one direction while the others conduct in the opposite direction. Note the steering diodes, which steer current around the nonconducting GTO, and the individual capacitor-diode-resistor snubber network on each individual GTO. Each GTO is rated at 4500 V, 2000 A. The GTOs were manufactured by General Electric Co. in Malvern, PA. The solid state circuit breaker is capable of operating with one set of GTOs lost, that is, failed shorted. The gate drive for each GTO is supplied by a dedicated high performance gate drive circuit, each of which are controlled from the solid state circuit breaker's control circuit. Fiber optics are used for communication between the control circuits and the various gate drivers. Fiber optics are also used as the communication means between the two solid state circuit breaker controls and the system controller.

The solid state circuit breaker control performs a variety of diagnostic functions and provides visual fault indications. The features are aids to identifying operational problems and/or defective power components. These controls and indicators are intrinsic to the solid state circuit breakers themselves and are in addition to the controls on the power supply control system.

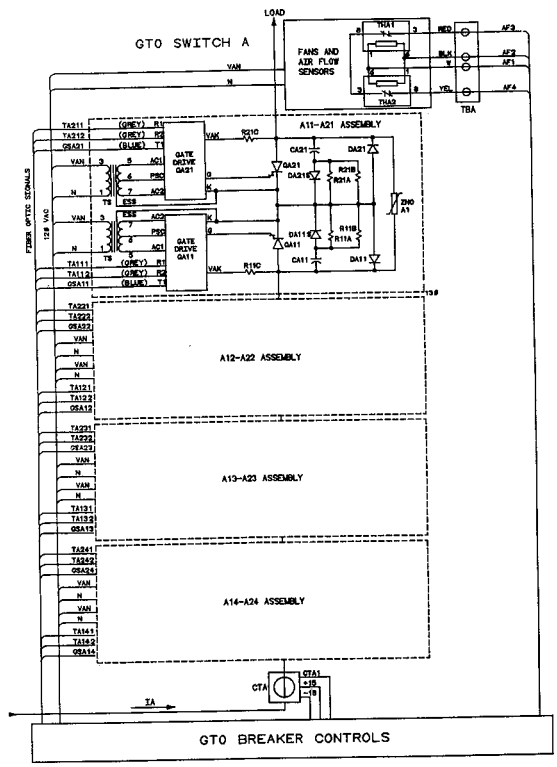

Figure 2. Schematic of one phase of solid state circuit breaker with detail of one assembly of antiparallel GTOs (A11-A21). Note the GTOs (QA21 and QA11), snubber circuits (DA21S, CA21S and R21 A and B, and DA11S, CA11S and R11 A and B), the steering diodes (DA21 and DA11) and overvoltage protection (ZN0A1).

Control and Data Acquisition

Each 3.3 MW power supply is turned on and off by a solid state circuit breaker, and its dc output is controlled by a Step Voltage Regulator (SVR). These devices, in turn, may be controlled from the power supply's existing, though now modified, control panel, or by a Macintosh computer running the National Instruments LabVIEW 2 program. There are, in turn, two modes of control by the computer; one is via the keyboard and the other is automatic. The keyboard mode allows the power supply operator to control the power supply using the keyboard and mouse of the computer. The automatic mode allows the use of preprogrammed instructions to control the power supply and therefore allows for unattended operation. Power supply status, output current, SVR position, and output voltage are always displayed on the manual control panel and, if the power supply is being run from the computer, these parameters are displayed on the computer monitor. The control system was designed and built by Maxwell Laboratories, San Diego, CA.

A hardwired fast power supply trip has been implemented as part of the controls. This function is performed by the Peak/Fault Detector. The Peak/Fault Detector monitors the voltage and current waveforms of the experiment and uses this information as a basis for issuing trip commands, when the power supply is being run from the computer. This device provides fast power supply shut off protection for experiment components. Up to four experiment waveforms can be monitored simultaneously, in real time, by the Peak/Fault Detector. Whenever any pre-selected combination of these monitored waveforms departs from "normal" by an amount defined by the operator, the Peak/Fault Detector commands the solid state circuit breaker to open. The response time of this action is less than 300 μs from the time of waveform departure until the ac current is interrupted. Figure 3 shows the hardware block diagram of the power supply control and data acquisition system.

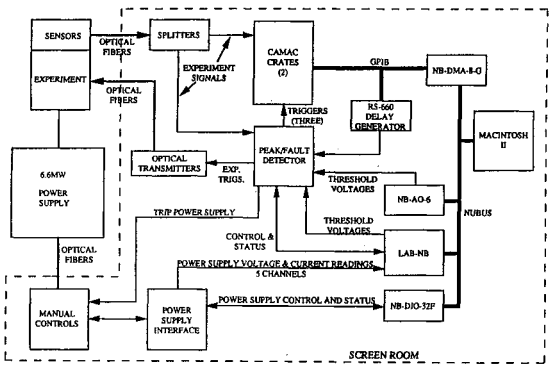

Figure 3. Power supply control and data acquisition system block diagram. The Peak/Fault Detector (center) provides a hardwire trip control based on experiment parameters being fed directly into the detector, and allowing the detector to trip the system without the use of the control computer (right). The detector is programmable from the computer, to "normal" waveform settings and will trip if one or more of the experiment wave forms deviates from normal. The control computer also controls the CAMAC based data acquisition system and system timing via the RS-660 delay generator (top).

The Peak/Fault Detector monitors the waveforms for faults and the CAMAC instruments digitize and store these waveforms.

The Manual Controls are implemented using a GE Fanuk programmable logic controller (PLC). A key switch on the front panel of the Manual Controls allows the operator to select manual control or computer control. The PLC and the Solid State Circuit Breaker have a handshaking protocol to assure reliable control of the Solid State Circuit Breaker. The Power Supply Interface provides ohmic isolation and voltage level changing for the digital signals and ohmic isolation for the power supply output voltage, output current and SVR position analog signals.

The RS-660 Delay Generator generates enable gates for the Peak/Fault Detector, trigger signals for the CAMAC instruments and trigger signals for the experiment. The experiment triggers and the CAMAC instrument triggers are passed through the Peak/Fault Detector, so that they may be interrupted in case of a waveform detected fault. The enable gate signals pass the outputs of waveform threshold comparators to latch circuits. If any threshold is exceeded at the time of the gate signal, the latch is set, indicating a fault. This fault signal, in turn, generates a trip signal for the experimental triggers, the power supply and the CAMAC instruments, provided the operator has selected such trips before the run was begun.

Both the keyboard and automatic modes of computer control were implemented using the LabVIEW 2. By using the LabVIEW virtual instrument feature, in which the operator constructs a control panel for the instrument on the computer monitor, the operator selects power supply control and data acquisiton control instructions from a built-in set and attaches execution times to them to form a preprogrammed sequence of commands for an experimental run. The operator also uses virtual instrument panels to set up the Peak/Fault Detector, CAMAC instrument, and RS-660 parameters. A virtual instrument panel, called the "Keyboard Run" panel, is used to allow the operator to control the power supply and data taking in the keyboard control mode.

Before the start of an experimental run, the operator selects the repetition rate and the relative delays of two experimental triggers, three CAMAC digitizer triggers, and the enable gate signals for the Peak/Fault Detector using the controls on the "Set-up" virtual instrument panels. All of the timing information is used to program the RS-660 delay generator, so that it will supply the proper timing signals, in the proper phase, within each experimental repetition period. In the same fashion, the thresholds are set in the Peak/Fault Detector, the set-up information is provided for the CAMAC instruments, and the operator selects power supply control and data acquisition control instructions from a displayed set, if the run is intended to be automatic. Finally, the operator fills out a run permissive checklist on the "Check List" virtual instrument panel and selects either "automatic run" or "keyboard run". After the run, a "Display Data" panel appears on the screen from which the operator may upload data from the CAMAC instruments and view it on an oscilloscope-like virtual instrument display.

The source code, written in LabVIEW 2, consists of approximately 350 virtual instruments and occupies approximately 12 megabytes of computer disk space.

System Performance Tests

The system installation was completed during the last quarter of 1992. At this time, it was subjected to acceptance testing, which we summarize now.

The first tests were done using the apparatus shown in Figure 4. The load was two water loads in series, with each load having a resistance of nominally 90-120 ohms, depending on water temperature. An ignitron was used to switch one water load out of the circuit, thus lowering the resistance of the circuit and increasing the current and simulating a fault. Load voltage and current were monitored using the detectors indicated in the figure.

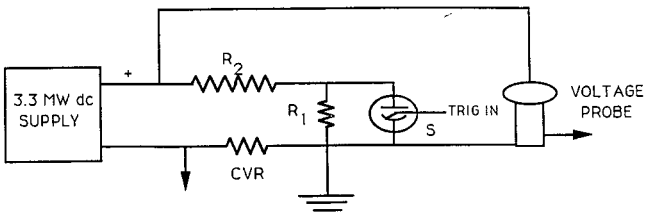

Figure 4. Test circuit for solid state circuit breaker.

After several cycling on and off tests, the power supply control circuit was set to trip at 400 A. The ignitron was then used to switch the current limiting resistor out of the circuit, causing a overcurrent and a trip of the solid state circuit breaker. The circuit breaker was tripped in one of two ways, the results of which are shown in Figure 5. The upper trace is a trip from the AC side of the power supply, and is accomplished in 200 microseconds. The second set of traces is on the DC side of the power supply, required signal processing and thus was slower in occurrence. It took 800 microseconds. This is still two orders of magnitude less than the time required by conventional mechanical circuit breakers.

a)

b)

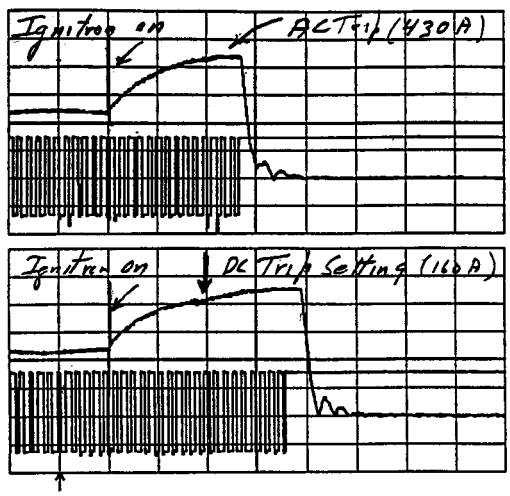

Figure 5. Power supply output under tripping conditions a) AC trip at 430 A. b) DC trip at 160 A setting. High frequency trace at bottom is enable signal for solid state circuit breakers. Lack of signal initiates trip in solid state circuit breaker. Vertical axis: 44 A/div, Horizontal axis 500 μs/div.

The above tests were performed in manual mode, off the existing, though modified, power supply control panel. The next step was to test the computer control. Tests similar to the above were performed. In addition, the system was tested for trips associated with additional faults, including:

- Prefire
- Inverse conduction
- Continuous conduction
- Missing pulse

Having satisfied the above tests, the system was declared operational at the beginning of 1993. It's first task was in the testing of the EEV CX 1776 thyratron tube. The circuit schematic is shown in Figure 6. For the scope of this presentation, it can be said that the tube was tested to its limits and survived. This was possible only because the solid state circuit breakers were there to protect the device under test during faults, which were numerous. It may be argued that the investment in the solid state circuit breaker system, which exceeded one million dollars, has been justified in the savings realized in this one series of component tests.

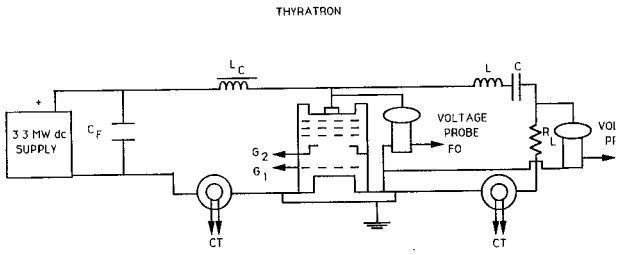

Figure 6. EEV CX 1776 thyratron test modulator.

Conclusion

The solid state circuit breakers are functioning now at the Army's Pulse Power Center. Their next task is the automated life testing of energy storage capacitors. The automated features of the power supply control system will make unattended, time intensive testing of pulse power components a reality, opening up new avenues in component reliability assurance and benchmarking in reasonable time.

Acknowledgment

The authors would be remiss if they did not acknowledge the contribution of Stephen Levy, currently of the Tennessee Valley Authority, who, as Chief of the Pulse Power Technology Branch at Fort Monmouth, conceived of the concept of a solid state circuit breaker, secured the initial funding for the project and who guided the project until the end of his tenure at Fort Monmouth. He continues to be an advocate of the technology, promoting it to the electric utility industry.